ABSTRACT

[0044] An exposed top end of a vertical oxide spacer is removed, and a nitride layer is deposited in an amount sufficient to replace the removed portion prior to exposing a memory device to a self align contact etch process. The nitride layer may be used to prevent a short circuit through the oxide spacer. The present invention also provides memory devices that have a gate stack, a vertical spacer adjacent to the gate stack, in which the vertical spacer has a lower portion comprising an oxide and an upper portion comprising a nitride, and a continuous nitride layer overlaying the vertical spacer and the gate stack. The present invention further provides methods of fabricating the above devices, and processor systems which include the devices.